

EDAptability adds cycle accurate Java model generator

Testbench/Design to timing/cycle accurate Java Model Transformer released

MUNICH, Germany, May, 26th, 2004 - EDAptability today announced its new timing/cycle accurate Java model generator. This new approach lifts verification and simulation to new heights. Assertions, Checkers, Random Verification, Design Debugger, Software Development Models and pre-compiled IP Objects are easier to handle using models in a common high level language like Java. Java has superb high level language elements, which are already partly adapted by other recently emerged EDA specific high level verification languages. Using a high level language as medium for more efficient verification techniques has already proven fruitful in the C/C++ domain.

The timing/accurate Java Models enable the verification engineer to use state of the art programming methods for the SoC verification. JavaVC (Java Verification Components) can be included to the simulation/verification environment. The combination of timing accurate testbench models and cycle accurate design models enable the engineer to use the environment as a platform independent license free simulator.

The current version of SynEDA 2.0 includes a mixed language (Verilog, VHDL) simulator HS and an RTL to C/Java Model Transformer CG/JG. The tool combines synthesis algorithms with simulation techniques. This approach makes the RTL simulation behave like the high level functional design representation after synthesis. The technology benefit comes from a central cycle accurate C/Java model of the design, as well as from the fact, that hardware and software developer can share the same C/Java model, which itself is a the high level functional design representation after synthesis.

Pricing and Availability

EDAptability's SynEDA 2.0 includes the mixed language simulator HS and the RTL to C/Java Model Transformer CG/JG.

The one-year-one-host license is priced at 3800 € and is available. Current customers get a free upgrade to SynEDA 2.0.

About EDAptability

EDAptability provides leading edge EDA tools for the complete ASIC and FPGA market. EDAptability's mixed language simulator and EDAptability's testbench/design to timing/cycle accurate C/Java Model Transformer enable the customer to close the Hardware-Software-Co-Development gap. Its state of the art technology enables the C-user to run the fastest possible simulation and shortens simulation and verification time significantly. For more information, visit www.EDAptability.com.

For more information contact:

Tobias Strauch

[EDAptability](http://www.EDAptability.com)

++49+89+21568547

tobias@EDAptability.com