

EDAptability: RTL-to-RTL partitioner released, including auto partitioning and timing driven algorithms

Enables RTL level post-simulation and incremental system prototyping flow

MUNICH, Germany, August, 2nd, 2007 - EDAptability today announced that it released its RTL-to-RTL partitioner to the public, after having tested it at early customer's projects. The partitioner is targeted for the system prototyping field. The methodology and tool features are based on the compiled experiences at various projects, applications, customers and system prototyping hardware.

It reads RTL source code as well as the board/system description file. The key difference to netlist (edif) based partitioning tools is that the source code is modified so that the output after the partitioning process is again available in the same original format. This enables RTL-level post simulation of the partitioned code using the original testbench. In case a bug was inserted, it can be analyzed on RTL level and no time consuming debugging on FPGA level is needed. Another key advantage is the possibility to synthesize each FPGA starting from RTL stand alone. In case one file changes, only the corresponding FPGA needs to be recompiled using incremental syntheses, place and route features of the FPGA-compiler.

The tool has an excellent GUI, which gives a great overview of the current status of the partitioning process. One benefit is the quick STA feature to see the current timing of the defined clock domains in the system. Besides that, the user can use the auto place and auto route features, which can be mixed with manual placement and routing and which also use the STA results to select the fastest auto partitioning result.

"In 10 years of working in the system prototyping field, I always made the observation, that the projects which are lucky to partitioning the code on RTL level with RTL-level simulation and FPGA-based incremental synthesis where much more successful and efficient than the one who spend a lot of time at netlist modification, netlist or FPGA debugging and hours of overall synthesis, place and route times over and over again. It follows the general trend to fix issues on RTL level and the effort by the FPGA-compiler provider to improve incremental features. I think this is a major milestone for the system prototyping area." said Tobias Strauch, developer at EDAptability.

For switch based system prototyping hardware, the switches are set/unset incrementally to reach the best routing result. Also new to the market is the integrated memory replacer. Instead of manually modify RTL code, the user can select potential memory signals, which are then replaced with the selected Altera or Xilinx memory macro on RTL level.

Pricing and Availability

EDAptability's SynEDA 3.0 partitioner feature includes the RTL-to-RTL partitioner with semi- or full- automated, timing driven partitioning.

The one-year-one-host license is priced at 8000 € and is available.

About EDaptability

EDaptability provides leading edge EDA tools for the complete ASIC and FPGA market. EDaptability's key technologies reach from unique simulator techniques to RTL-to-RTL partitioner techniques as well as outstanding system prototyping hardware. Each component can be seen as ahead of the competitors and gives direct benefit to the customer. For more information, visit www.EDaptability.com.

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